GEORGIOS E.N. KORNAROS

Assistant Professor
Department of Informatics Engineering
Technological Educational Institute of Crete
Estavromenos 71004, Iraklio, Crete, Greece
Tel.: +30 2810 379868, +30 2810 379168
Fax: +30 2810 371994
kornaros@ie.teicrete.gr

9 Akrokorinthou St
71409, Iraklio
Crete, Greece
Tel: +30 6976085743

kornaros@gmail.com

Research Interests

Multi/many-core architectures, high-speed communication architectures, embedded and reconfigurable systems, full and semi-custom IC design and methods

Research Synopsis

I originally worked on semi-custom and full-custom VLSI design, where I contributed initially to the front- and back-end design of Telegraphos-II switch chip and later to the design, characterization and implementation of multi-ported memories RAM and CAM for the ATLAS single-chip switch. In ISD SA I leaded the Digital Integrated Systems Group doing research and development of network processor architectures. In Ellemedia Technologies Ltd I worked in three (EU and national) projects as technical manager and co-head architect in the same domain of designing single-chip high-speed network processors. As appointed at TEI Crete, currently as Ass. Prof., the research activities focused on designing embedded systems for the Point-of-Care device in EU-funded project (Micro^{2}DNA) and developing Lab-on-Chip in national project (EPAN-II). The present research involves multi-core and heterogeneous architectures and particularly hardware support for optimizing embedded and cyber-physical systems with full-virtualization in terms of adaptable and secure processing (EU projects VIRTICAL, SAVE, TRESCCA, DREAMS, TAPPS).

EDUCATION

- University of Crete, Department of Computer Engineering and Electronics, Chania, Greece.
  Ph.D (Dec/2013)
  Thesis: “Real-time ASIC Monitoring for System-level Power and Thermal Management”

- University of Crete, Department of Computer Science, Heraklion, Greece.
  M.Sc. in Computer Science (Jun/1997). GPA 8.5/10.0
  Areas: Computer Architecture, VLSI design, High-Speed Networks and Communication Architectures.
  Thesis: “Implementation of Pipelined Multi-Queue Management in the ATLAS I Switch in Full-Custom CMOS VLSI”

- University of Patras, Department of Computer Engineering & Informatics, Patra, Greece.
  Diploma in Computer Engineering and Informatics (Jun/1992). GPA 8.53/10.00

EXPERIENCE (Appointments – Projects)

6/2015 - now Assistant Prof. - Informatics Engineering Department (formerly Applied Informatics and Multimedia Department) – Technological Educational Institute of Crete (TEI) **(**3/2006 – 5/2015 Lecturer**)**
Head/Director of Intelligent Systems & Computer Architecture Lab (ISCA Lab) (Apr.2016 - now)

- Teaching Undergraduate Courses: Computer Architecture, Digital Design, System Digital Design with FPGAs, Microcontrollers/Microprocessors, Embedded Systems
- Teaching Graduate Courses: Multi-core Architectures, Advanced Embedded System Design

1/01/2015 – 31/12/2017 TEI Crete Scientific Coordinator – EU/H2020 Project acronym: **TAPPS**, Project full title: “Trusted Apps for Open CPS", Grant agreement no: 645119, H2020-ICT-01-2014 Smart Cyber-Physical Systems (EU Funding 3,885,484 €) (H2020-ICT/RIA/TAPPS 645119)
TAPPS is a Research and Innovation Action (RIA) European project which provides and validates an end-to-end solution for development and deployment of trusted apps, including an App Store and a model-based tool chain for trusted application development. The role of TEI is to extend the execution environment inside the System Control Units and exploit functionalities provided by the novel hardware-, processor- and network-centric security mechanisms for on-chip and off-chip communications. http://www.tapps-project.eu/

1/09/2013 – 1/09/2016 TEI Crete Scientific Coordinator – EU/FP7 Project acronym: **SAVE**, Project full title: "Self-Adaptive Virtualisation-Aware High-Performance/Low-Energy Heterogeneous System Architectures", Grant agreement no: 610996, FP7-ICT-2013-10 (EU Funding 2,930,000 €) (FP7-ICT/STREP/SAVE 610996)

SAVE is a European collaborative research project funded within the Seventh Framework Programme (FP7) aimed at the development of software/hardware technologies for an efficient exploitation of *heterogeneous system architectures*. In the SAVE project HW/SW/OS components are developed that allow for deciding at runtime the mapping of the computation kernels on the appropriate type of resource, based on the current system context and requirements. http://www.fp7-save.eu/ (The project launched in September 2013 and has 36 months duration.)

1/10/2012 – 1/10/2015 Member – EU/FP7 Project acronym: **TRESCCA**, Project full title: "TRustworthy Embedded systems for Secure Cloud Computing Applications", Grant agreement no: 318036 Collaborative project FP7-ICT-2011-8 (EU contribution: 2,950,000 €)

The TRESCCA project aims to lay the foundations of a secure and trustable cloud platform by ensuring strong logical and physical security on the edge devices, using both hardware security and virtualization techniques while considering the whole cloud architecture. http://www.trescca.eu/index.php. (01/10/2012-30/09/2015)

1/10/2013 – 1/10/2017 Member – EU/FP7 Project acronym: **DREAMS,** Project full title: "Distributed REal-time Architecture for Mixed Criticality Systems" (FP7-ICT IP DREAMS 610640)

The objective of DREAMS is to develop a cross-domain architecture and design tools for networked complex systems where application subsystems of different criticality, executing on networked multi-core chips, are supported. DREAMS will deliver architectural concepts, meta-models, virtualization technologies, model-driven development methods, tools, adaptation strategies and validation, verification and certification methods for the seamless integration of mixed-criticality to establish security, safety, real-time performance as well as data, energy and system integrity.

DREAMS is one of three projects funded by the European Commission in the area of mixed-criticality systems from the FP7 ICT call 10. The EC financial contribution amounts to 11 million euros.

http://www.dreams-project.eu/

15/07/2011 – 15/07/2014 TEI Crete Scientific Coordinator – EU/FP7 Project acronym: **VIRTICAL**, Project full title: "SW/HW extensions for virtualized heterogeneous multicore platforms ", Grant agreement no: 288574 Theme [ICT-2011.3.4: Computing Systems] (EU Contribution: 2,860,000 €)

The vIrtical project aims to increase functionality, reliability and security of embedded devices at sustainable cost and power consumption. This is achieved in the vIritical project by extending the virtualization concept of the general-purpose domain to the embedded domain. In order to expand the virtualization concept to the embedded devices, this project will deliver software/hardware extensions at different layers of the design stack (hardware, operating system, hypervisor and applications) to increase flexibility, programmability, performance, QoS, reliability, security and power saving. http://www.virtical.eu/

1/06/2012 – 1/06/2015 Member of Main Research Team – "Application Specific Hierarchical Shared Memory (ASHSHMEM)", Υποέργο 31 με τίτλο «Ιεραρχικά Κοινόχρηστα Συστήματα Μνήμης για Ενσωματωμένες Εφαρμογές» στο πλαίσιο της πράξης "ΑΡΧΙΜΗΔΗΣ ΙΙΙ - ΕΝΙΣΧΥΣΗ ΕΡΕΥΝΗΤΙΚΩΝ ΟΜΑΔΩΝ ΣΤΟ ΤΕΙ ΚΡΗΤΗΣ" Χρηματοδοτικός φορέας: ΕΠΕΔΒΜ- Επιχειρησιακό Πρόγραμμα "Εκπαίδευση και Δια Βίου Μάθηση" (Συνολικός προϋπολογισμός: 82 k€)

10/2009 – 09/2010 TEI Crete Scientific Coordinator – "Στοιχεία Μικροηλεκτρονικής για Lab-On-Chip Όργανα Μοριακών Αναλύσεων για Γενετικές και Περιβαλλοντικές Εφαρμογές"- Lab-On-Chip-ATEI-CRETE, Corallia Microelectronics Cluster, ΜΙΚΡΟ2-39/Ε-ΙΙ-Γ, Φάση-2 Ενίσχυσης Ελληνικών Τεχνολογικών Συνεργατικών Σχηματισμών στη Μικροηλεκτρονική/ΜΙΚΡΟ2-ΣΕ-Γ/Ε-ΙΙ, Ε.Π. Ανταγωνιστικότητα και Επιχειρηματικότητα (ΕΠΑΝ-ΙΙ) – Π.Ε.Π. Περιφερειών Μεταβατικότητας Στήριξης (συνολικού προϋπολογισμού 3,084,885 €), 1/10/2009-31/12/2012

6/2006 – 6/2009 Center for Research & Technology TEI Crete – **EU/FP6** Project acronym: **Micro2DNA**

- Worked under the FP6-IST-4-027333-STP project Micro^{2}DNA "Integrated polymer-based micro-fluidic micro-system for DNA extraction, amplification, and silicon-based detection", designing the electronic part of the embedded system for the Point-of-Care device.

5/2001 – 12/2005 Employed by *Ellemedia Technologies*, Athens.
Founder and Technical Manager of the Ellemedia Technologies Crete Department

- Working on WEBSoC (GSRT Project), a network processor on a VirtexII-Pro FPGA responsible for Queue Management and Scheduling components, and chip integration. - EUREKA E!3326 WEBSoC (Wireless Ethernet Bridging System-on-Chip)
- Working on NP-MADE on hardware scheduler and traffic shaper components. - EUREKA E!3132 NP-MADE (Network Processor for Multi-service Access Devices)
- Previously worked on *PRO3* (the Protocol Processor Project, IST 11499), a single chip network processor (fabricated with a standard 0.18um cmos technology by UMC), as hardware designer of the Scheduler sub-blocks. Architectural design, implementation, and synthesis of Scheduling Components and memory interfaces.

2/2000 – 4/2001 Employed by *Integrated Systems Development (**ISD**)*, Athens
Technical Manager of the Digital Integrated Systems Group, **Founder** of ISD-Crete Dept.

- **ISD** collaborates with France based **SGS Thomson Microelectronics** (ST Microelectronics) developing IPs for Telecom applications, memories for Low-Power devices and methodology for embedded system verification. Managed the development of BroadBand Network Terminal (BBNT), specifying the architecture and verification methodology in collaboration with the AST – ST group. BBNT is a system on chip, combining 8 physical ATM links of aggregate bandwidth 155 Mbps, 8 Ethernet 10/100 links, and supporting multiple protocols (ATM, AAL0, AAL5, Ethernet switching, VLAN and DIX support, IP over ATM, MPOA, LANE v1 and v2) with the aid of embedded CPU cores.

- Consulting services to CARV group (Computer Architecture & VLSI) of the Computer Science Institute, Foundation of Research and Technology, Heraklio (FORTH), regarding network architectures and VLSI design.

1/1999 – 6/2000 Employed by *Institute of Computer Science, Foundation of Research & Technology* (***ICS – FORTH***), Heraklion

- Member of Computer Architecture and VLSI systems group (CARV). Worked on ATLAS-II, an optimized version of ATLAS, a 16x16 single chip ATM switch. In Front-End (FE) using Synopsys tools, Verilog and Verisure, optimized sub-blocks of ATLAS. In Back-End (BE) compacted ATLAS to nearly 50% using full-custom design techniques whenever beneficial. Used Unicad Design Kit under Cadence DFWII, Silicon Ensemble.

3/1998 – 12/1998

- Worked under the ASICCOM project, integrating ATLAS and performing the placement and routing of the chip, as well as the verification (DRC, ERC, LVS). Used extensively Preview Cell3 Ensemble, CELL3, Silicon Ensemble, Cadence DIVA/DRACULA verification products, Unicad Tools (by SGS-Thomson). ATLAS I is a 16x16 single chip ATM switch that provides advanced flow control (multilane back-pressure), a large on-chip cell buffer (256 cells), aggregate bandwidth of 10Gb/s and supports three priority levels, multiple logical queues and efficient multicasting. ATLAS I was designed in a 0.35micron CMOS process using 6 million transistors, and was taped-out for fabrication on November 1998.

6/1996 – 3/1998

- Designed the queue management subsystem of ATLAS switch, implementing three-ported and four-ported SRAMs, CAM blocks Priority Enforcer and peripheral circuits in full-custom VLSI.
- Characterized the full-custom blocks of ATLAS and developed verilog models (**8/97 – 3/98)**.
  Used Analog Artist, Virtuoso Layout Editor, Spice, Hspice, Anacad Tools (ELDO, Xelga), Verilog.

6/1994 – 5/1995

- As a member of the CARV group designed and implemented Telegraphos II Switch (Semi-Custom Design with ES2 CMOS ecpd07 0.7um process), a single switch chip with four-by-four unidirectional point-to-point links, providing 1.2 Gbps aggregate throughput with DDR techniques, and featuring shared buffering, virtual circuit (VC) level, credit-based flow control, and cut-through.
- Used Verilog, ES2 design kit under the Cadence DFW. Telegraphos is a project to design architectures and build prototypes for high speed computer communication, in Networks of Workstations or Workstation Clusters.

ACTIVITIES

Organizations - Presentations

[1] DATE 2017 Tutorial "The Internet of INSECURE Things", Organizer: Marcello Coppola, STMicroelectronics, FR, George Kornaros, TEICrete, GR, Giovanni Gherardi, Energica Motor Company, IT, Presentation: G. Kornaros, "Using a Secure IoT Platform Based on STM32 MCUs"

[2] IEEE/ACM Design, Automation and Test in Europe (DATE) 2013, Embedded Tutorial: "From Embedded Multi-core SoCs to Scale-out Processors", Marcello Coppola, Babak Falsafi, John Goodacre, George Kornaros, March 20, 2013

[3] HiPEAC 2014, January 20-22, 2014 | Vienna Austria Workshop/Tutorial VVITEMES, "First Workshop on Vertical Virtualization Techniques in Heterogeneous Multicore Embedded Systems", María Engracia Gómez, Andrea Marongiu, Sergey Tverdyshev, Marcello Coppola, Georges Kornaros, Davide Bertozzi and José Flich

[4] IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2010 Heraklion, Greece, July 8-9, 2010, Conference Co-Chairman – Organizer (M. Grammatikakis – G. Kornaros)

[1] Reviewer, ACM Journal on Emerging Technologies in Computing Systems, Mar 2018
[2] Reviewer, Journal: Microprocessors and Microsystems, Dec 2017 Elsevier B.V.
[3] Reviewer: IEEE Transactions on VLSI (Oct'17)
[4] Reviewer: IEEE Transactions on Multi-Scale Computing Systems (2017)
[5] Reviewer: Journal JLPEA (ISSN 2079-9268), http://www.mdpi.com/journal/jlpea/special_issues/embedded_systems
[6] Program Committee in Mobile Networks for Biometric Data Analysis (mBiDa 2014)
[7] Reviewer, ACM TODAES, 2014
[8] Reviewer, IEEE Transaction on Parallel and Distributed Systems (IEEE TPDPS), 2013
[9] Reviewer, IEEE Transaction on Computers (IEEE TC), 2012
[10] Reviewer, Elsevier JSA, 2012
[11] Reviewer, ACM TRETS, 2013
[12] Reviewer, CRC Press (www.crcpress.com), Series: Embedded Multi-Core Systems
[13] Participation in IPEAI - The Intensive Programme on Embedded and Ambient Intelligence, Lifelong Learning Programme (LLP) – Erasmus Action, 26 July - 6 August, 2010, Aveiro, Portugal
[14] IPEAI - The Intensive Programme on Embedded and Ambient Intelligence, Lifelong Learning Programme (LLP) – Erasmus Action, 18 July - 1 August, 2009, Kiel, Germany
[15] Reviewer, IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2011, Regensburg, July 7-8, 2011, 2012, 2013
[16] IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2010 Heraklion, Greece, July 8-9, 2010
Conference Co-Chairman – Organizer
[17] Reviewer, ASIC/SOC Conference 2011
[18] Reviewer, Design, Automation and Test in Europe Conference (DATE'2010)
[19] IEEE Workshop on Intelligent Solutions in Embedded Systems – WISES2009 Ancona, Italy, June 25-26, 2009
Session Chairman
[20] DSD'2003 EUROMICRO Symposium on Digital System Design, Architectures, Methods and Tools, Antalya, Turkey, September 3 – 5, 2003
Session Chairman

PATENTS
[1] Filing:

United Kingdom	26 May 2017	1708464.1	82615001	Application	
United States of America			82615026	Acknowledged	

Title: "APPARATUS FOR USE IN A CAN SYSTEM"
Greek Application No. 20170100160, filed on April 5, 2017
Inventors Antonio-Marcello Coppola, Georgios Kornaros, Giovanni Gerardi
Original Assignee Stmicroelectronics (Grenoble 2) Sas, Technological Educational Institute of Crete, Energica S.p.A.

[2] "**Apparatus and methods implementing dispatch mechanisms for offloading executable functions**"
Publication number US20170206169 A1
Publication type Application
Application number US 15/402,515
Publication date Jul 20, 2017
Filing date Jan 10, 2017
Priority date Jan 15, 2016
Inventors Antonio-Marcello Coppola, Georgios Kornaros, Miltos Grammatikakis
Original Assignee Stmicroelectronics (Grenoble 2) Sas, Technological Educational Institute of Crete
https://www.google.com/patents/US20170206169

[3] "**Resource access control in a system-on-chip**"
Publication number US9519596 B2
Publication type Grant
Application number US 14/629,613

Publication date Dec 13, 2016
Filing date Feb 24, 2015
Priority date Mar 6, 2014
Also published as US20150254189
Inventors Antonio-Marcello Coppola, Georgios Kornaros, Miltos Grammatikakis
Original Assignee Stmicroelectronics (Grenoble 2) Sas, Technological Educational Institute of Crete
https://www.google.com/patents/US9519596

[4] Inventor(s): Antonio-Marcello COPPOLA. George Kornaros. Miltos Grammatitakis.
Title : **"System Address-Space Protection/Security Service Support at the Network-on-Chip"**
Application for patent has been filed on 06 Mar 2014, Invention Ref: 13-GR2CO-0333.

PUBLICATIONS

Journals

[1] Dimitrios Mbakoyiannis, Othon Tomoutzoglou, and George Kornaros. 2018. Energy-Performance Considerations for Data Offloading to FPGA-Based Accelerators Over PCIe. ACM Trans. Archit. Code Optim. 15, 1, Article 14 (March 2018), 24 pages. DOI: https://doi.org/10.1145/3180263

[2] Ioannis Christoforakis, Maria Astrinaki, and George Kornaros. 2018. Towards architectural support for bandwidth management in mixed-critical embedded systems. SIGBED Rev. 14, 4 (January 2018), 21-26. DOI: https://doi.org/10.1145/3177803.3177807

[3] Miltos D. Grammatikakis, Kyprianos Papadimitriou, Polydoros Petrakis, Antonis Papagrigoriou, George Kornaros, Ioannis Christoforakis, Othon Tomoutzoglou, George Tsamis, Marcello Coppola, "**Security in MPSoCs: A NoC Firewall and an Evaluation Framework**", IEEE Trans. on CAD of Integrated Circuits and Systems, vol 34 – 8, pp.1344-1357, 2015, DOI: 10.1109/TCAD.2015.2448684

[4] G. Kornaros and D. Pnevmatikatos, "**Dynamic Power and Thermal Management of NoC-based Heterogeneous MPSoCs**", *ACM Transactions on Reconfigurable Technology and Systems* (TRETS), Volume 7 Issue 1, February 2014 Article No. 1, 26 pages. DOI=10.1145/2567658 http://doi.acm.org/10.1145/2567658

[5] Georgios Kornaros and Dionisios Pnevmatikatos. 2013. **A Survey and Taxonomy of on-Chip Monitoring of Multi-core Systems-on-Chip**. *ACM Trans. Des. Autom. Electron. Syst.* 18, 2, Article 17 (April 2013), 38 pages. http://doi.acm.org/http://dx.doi.org/10.1145/2442087.2442088

[6] G. Kornaros, "**High-Speed Hardware Arbitration Supporting Priorities and Bounded Service Latency**," *IEEE Embedded Systems Letters*, vol. 5, issue 2, pp. 21-24, Mar. 2013 doi: 10.1109/LES.2013.2251454, issn: 1943-0663 http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6475963&isnumber=5170179

[7] George Kornaros and Theofanis Orfanoudakis, "**Design and Implementation of High-Speed Buffered Crossbars with efficient Load Balancing for Multi-Core SoCs**", J. Microprocessors and Microsystems (2010), DOI information: 10.1016/j.micpro.2010.06.002 Microprocessors and Microsystems, Volume 34, Issues 7-8, November 2010, Pages 301-315, Elsevier Science Publishers B. V., doi:10.1016/j.micpro.2010.06.002

[8] George Kornaros, "**NCXplore: a Design Space Exploration Framework of Temporal Encoding for on-chip Serial Interconnects**", International Journal of High Performance Systems Architecture (IJHPSA), Special Issue on: "Power-Efficient, High Performance General Purpose and Application Specific Computing Architectures", *Int. J. High Performance Systems Architecture, Vol. 2, Nos. 3/4, 2010*

[9] George Kornaros, "**A Soft Multi-core Architecture for Edge Detection and Data Analysis of Microarray Images**", J. Syst. Architect. JSA (2009), Volume 56, Issue 1, January 2010, Pages 48-62, Elsevier Science Publishers B. V., http://dx.doi.org/10.1016/j.sysarc.2009.11.004

[10] *G. Kornaros, A. Demiris* and *S. Blionas*, **"Lab-on-Chip for Pharmacogenomics: An Embedded System Organization",** Micro and Nanosystems, Volume 1, Number 1, March 2009 , pp. 30-40, ISSN: 1876-4029 (Print), ISSN: 1876-4037 (Online)

[11] George Kornaros, Matthias Sund, Wolfram Lautenschlaeger, Helen-Catherine Leligou, and Theofanis Orphanoudakis, "**Efficient Implementation of a Frame Aggregation Unit for Optical Frame-based Switching**", Elsevier AEÜ – International Journal of Electronics and Communications, ISSN: 1434-8411, vol. 64, no. 1, 2010, pp 17-28. - **AEU - International Journal of Electronics and Communications**, Volume 64, Issue 1, January 2010, Pages 17-28, Elsevier Science Publishers B. V.

[12] G. Kornaros and S. Blionas, "**Microarchitecture of a MultiCore SoC for Data Analysis of a Lab-on-Chip Microarray**", *EURASIP Journal on Advances in Signal Processing*, vol. 2008, Article ID 520641, 11 pages, 2008. doi:10.1155/2008/520641.

[13] J. D. Angelopoulos,, K. Kanonakis, H. C. Leligou, Th. Orphanoudakis, G. Kornaros, "**Multiplexing QoS-Differentiated Traffic in an Ethernet-based Access Network**", The Mediterranean Journal of Computers and Networks, Vol. 4, No. 2, 2008

[14] Y. Papaefstathiou , S. Perissakis, D. Pnevmatikatos, G. Kornaros, F. Orphanoudakis, N. Nikolaou, K. Pramataris, K. Vlachos, G. Konstantoulakis, N. Zervos, "**PRO3: A Hybrid NPU Architecture**", **IEEE Micro**, vol.24, No.5, year 2004, pp 20-33, http://doi.ieeecomputersociety.org/10.1109/MM.2004.55

[15] A. Nikologiannis, G. Kornaros, I. Papaefstathiou, C. Kachris , "**An FPGA-based Queue Management System for High Speed Networking Devices**", Elsevier Journal: **Microprocessors and Microsystems**, Volume 28, Issues 5-6, Pages 193-350 (2 August 2004) Special Issue on FPGAs: Applications and Designs, pages 223-236 http://www.elsevier.com/locate/micpro

[16] Georgios Kornaros, Dionisios Pnevmatikatos, Panagiota Vatsolaki, Georgios Kalokerinos, Chara Xanthaki, Dimitrios Mavroidis, Dimitrios Serpanos, Manolis Katevenis: ''**ATLAS I: Implementing a single-chip ATM switch with backpressure**", **IEEE Micro**, 19(1), January/February 1999.

Edited Books

[1] G. Kornaros (Editor) *Multi-Core Embedded Systems*, CRC Press/Taylor & Francis Group, 07-April-2010, ISBN: 978-1-4398-1161-0, 501 pages.

[2] M.D. Grammatikakis, G. Kornaros, and N. Papadakis (Eds.), Proc. 8th Workshop on Intelligent Solutions in Embedded Systems (WISES2010), Heraklion, Greece, 2010. IEEE Catalog No: CFP10848-PRT/ART.

Book Chapters

[1] George Kornaros, Ernest Wozniak, Oliver Horst, Nora Koch, Christian Prehofer, Alvise Rigo, Marcello Coppola, "Secure and Trusted Open CPS Platforms", in book "Handbook of Research on Solutions for Cyber-Physical Systems Ubiquity", Editors: Norbert Druml, Andreas Genser, Armin Krieg, Manuel Menghin and Andrea Hoeller, IGI Global book series Advances in Systems Analysis, Software Engineering, and High Performance Computing (ASASEHPC) (ISSN: 2327-3453; eISSN: 2327-3461), 2017

[2] Miltos D. Grammatikakis, Marcello Coppola and George Kornaros, "The Spidergon STNoC", Book Chapter , Eds K. Tatas, K. Siozos, D. Soudris and Axel Jantsch, In "Designing 2D and 3D Network-on-Chip Architectures", Springer Science & Business Media New York 2014, ISBN 978-1461442738

[3] Miltos D. Grammatikakis, George Kornaros, Marcello Coppola, "Power-Aware Multicore SoC and NoC Design", Multiprocessor System-on-Chip, 2011, **Book Chapter 8**, pp 167-193, Eds Michael Hübner , Jürgen Becker, © Springer, Print ISBN 978-1-4419-6459-5, Online ISBN 978-1-4419-6460-1, DOI 10.1007/978-1-4419-6460-1_8, ISBN 978-1-4419-6459-5

[4] George Kornaros, "Energy Efficient Data Transmission of on-Chip Serial Links", in "Solutions on Embedded Systems", **Book Chapter 19**, Eds. Massimo Conti, Simone Orcioni, Natividad Martinez Madrid, Ralf E.D.Seepold, Springer, Series: Lecture Notes in Electrical Engineering (LNEE), ISBN 978-94-007-0637-8, 1st edition, 275p, 2011

[5] G. Kornaros, "Application Specific Customizable Embedded Systems", **Book Chapter 2**, 39 pages, in "Multi-Core Embedded Systems", Eds. G.Kornaros, CRC Press/Taylor & Francis Group, Apr. 2010, ISBN: 978-1-4398-1161-0.

[6] G. Kornaros, D. Pnevmatikatos, and Y. Papaefstathiou, "Monitoring Services for Networks-on-Chip", **Book Chapter 8**, 32 pages, in "Networks-on-Chips: Theory and Practice" Eds: Fayez Gebali, Haytham Elmiligi, and M. Watheq El-Kharashi, CRC Press, ISBN: 9781420079784, ISBN 10: 1420079786, March 25, 2009, 389 pages.

Conferences (refereed)

[1] George Kornaros and Svoronos Leivadaros, "Securing Dynamic Firmware Updates of Mixed-Critical Applications", 3rd IEEE International Conference on Cybernetics (CYBCONF), 2017, pp. 1-7, doi:10.1109/CYBConf.2017.7985807

[2] Christian Prehofer, Oliver Horst, Riccardo Dodi, Arjan Geven, George Kornaros, Eleonora Montanari, Michele Paolino, "Towards Trusted Apps platforms for open CPS", 3rd International Workshop on Emerging Ideas and Trends in Engineering of Cyber-Physical Systems, (EITEC, CPSWeek0, 2016, Vienna, Austria, April 11, 2016, pp. 23-28, DOI: 10.1109/EITEC.2016.7503692

[3] George Kornaros and Menelaos Pratikakis, "VWQS: A dispatching mechanism of variable-size tasks in heterogeneous systems", International Conference on High Performance Computing & Simulation, HPCS 2016, Innsbruck, Austria, July 18-22, 2016, pp. 196-203, DOI: 10.1109/HPCSim.2016.7568335

[4] Ioannis Deligiannis, George Kornaros, "Adaptive memory management scheme for MMU-less embedded systems", 11th IEEE Symposium on Industrial Embedded Systems, SIES 2016, Krakow, Poland, May 23-25, 2016, pp. 254-261, DOI: 10.1109/SIES.2016.7509439

[5] George Kornaros, Ioannis Christoforakis, Othon Tomoutzoglou, Dimitrios Bakoyiannis, Kallia Vazakopoulou, Miltos Grammatikakis, Antonis Papagrigoriou, "Hardware Support for Cost-Effective System-Level Protection in Multi-core SoCs.",

2015 Euromicro Conference on Digital System Design, DSD 2015, Madeira, Portugal, August 26-28, 2015, pp. 41-48, DOI: 10.1109/DSD.2015.65

[6] Christian Prehofer, George Kornaros, Michele Paolino, “TAPPS - Trusted Apps for Open Cyber-Physical Systems.”, E-Democracy - Citizen Rights in the World of the New Computing Paradigms - 6th International Conference, E-Democracy 2015, Athens, Greece, December 10-11, 2015, Proceedings, pp. 213-216, DOI: 10.1007/978-3-319-27164-4_18

[7] Ioannis Christoforakis, Othon Tomoutzoglou, Dimitrios Bakoyiannis, George Kornaros, “Dithering-Based Power and Thermal Management on FPGA-Based Multi-core Embedded Systems.”, 13th IEEE International Conference on Embedded and Ubiquitous Computing (EUC), Porto, Portugal, October 21-23, 2015, pp. 173-177, DOI: 10.1109/EUC.2015.18

[8] Miltos D. Grammatikakis, Antonis Papagrigoriou, Polydoros Petrakis, Kostas Harteros, George Kornaros, “Load balancing, broadcast, and scatter primitives for efficient multicore applications.”, 12th International Workshop on Intelligent Solutions in Embedded Systems, WISES 2015, Ancona, Italy, October 29-30, 2015, pp. 23-28

[9] Miltos D. Grammatikakis, Polydoros Petrakis, Antonis Papagrigoriou, George Kornaros, Marcello Coppola, “High-level security services based on a hardware NoC Firewall module.”, 12th International Workshop on Intelligent Solutions in Embedded Systems, WISES 2015, Ancona, Italy, October 29-30, 2015, pp. 73-78

[10] G. Durelli, M. Coppola, K. Djafarian, G. Kornaros, A. Miele, M. Paolino, O. Pell, C. Plessl, M.D. Santambrogio, and C. Bolchini, “SAVE: Towards efficient resource management in heterogeneous system architectures”, 10th International Symposium on Reconfigurable Computing: Architectures, Tools, and Applications, ARC 2014, Lecture Notes in Computer Science, Volume 8405 LNCS, 2014, Pages 337-344

[11] M. Grammatikakis, K. Papadimitriou, P. Petrakis, A. Papagrigoriou, G. Kornaros, I. Christoforakis, and M. Coppola, “Security Effectiveness and a Hardware Firewall for MPSoCs,” in IEEE International Conference on High Performance Computing and Communications (HPCC), to appear, August 2014.

[12] I. Christoforakis, O. Tomoutzoglou, D. Bakoyiannis and G. Kornaros, "Runtime Adaptation of Embedded Tasks with a-priori known Timing Behavior Utilizing On-line Partner-Core Monitoring and Recovery", in Proceeding of the 12th IEEE International Conference on Embedded and Ubiquitous Computing (EUC'2014), Milan, Aug 2014

[13] Marcello Coppola, Miltos Grammatikakis, George Kornaros, Alexander Spyridakis, “ Trusted Computing on Heterogeneous Embedded Systems-on-Chip with Virtualization and Memory Protection”, The Fourth International Conference on Cloud Computing, GRIDs, and Virtualization, CLOUD COMPUTING 2013, May 27 - June 1, 2013 - Valencia, Spain

[14] George Kornaros, Kostantinos Harteros, M. Astrinaki, I. Christoforakis, Marcello Coppola, M. D. Grammatikakis, “An IOMMU for hardware-assisted full virtualization of heterogeneous multicore SoCs”, VLSI Circuits and Systems VI, SPIE Microtechnologies, 24 - 26 April 2013, Alpexpo, Grenoble, France

[15] Marcello Coppola, John Goodacre, George Kornaros, Babak Falsafi , Embedded Tutorial: “From multi-core SoC to scale-out processors”, DATE, Mar. 2013, pp. 947-951

[16] George Kornaros, Miltos D. Grammatikakis, Marcello Coppola, “Towards Full Virtualization of Heterogeneous NoC-based Multicore Embedded Architectures”, 10th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (IEEE/IFIP EUC 2012) (invited)

[17] Kornaros, G., Pnevmatikatos, D., “Real-time monitoring of multicore SoCs through specialized hardware agents on NoC network interfaces”, *Proceedings of the 2012 IEEE 26th International Parallel and Distributed Processing Symposium Workshops, IPDPSW 2012* , RAW, art. no. 6270646 , pp. 248-255

[18] Kornaros, G., Christoforakis, I.,Astrinaki, M., “An automated infrastructure for real-time monitoring of multi-core systems-on-Chip”, *Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2012* , art. no. 6219025 , pp. 56-61

[19] A. Motakis, G. Kornaros, M. Coppola, “Dynamic Resource Management in Modern Multicore SoCs by Exposing NoC Services”, IEEE, 6th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC’2011), Montpellier, France, Jun. 20-21, 2011.

[20] G. Kornaros, D. Pnevmatikatos, “Hardware-assisted Dynamic Power and Thermal Management in Multi-core SoCs”, IEEE 21st Great Lakes Symposium on VLSI (GLSVLSI 2011), EPFL, Lausanne, Switzerland, 2-4 May 2011, pp 115-120. (acceptance rate 27%)

[21] George Kornaros, Antonios Motakis, "On Scaling Speedup with Coarse-Grain Coprocessor Accelerators on Reconfigurable Platforms," Digital Systems Design, Euromicro Symposium on, pp. 355-362, 2010 13th Euromicro Conference on Digital System Design: Architectures, Methods and Tools, 2010

[22] George Kornaros, “Temporal Coding Schemes for Energy Efficient Data Transmission in Systems-on-Chip”, in Proceedings of IEEE Workshop on Intelligent Solutions in Embedded Systems Ancona, Italy, June 25-26, 2009. **Best Paper Award**.

[23] George Kornaros, Wolfram Lautenschlaeger, Matthias Sund, and Helen-Catherine Leligou, “Architecture and Implementation of a Frame Aggregation Unit for Optical Frame-based Switching”, International Conference on Field Programmable Logic and Applications (FPL), Heidelberg, Germany, September 08-10, 2008, On page(s): 639-642, ISBN: 978-1-4244-1960-9, Digital Object Identifier: 10.1109/FPL.2008.4630028

[24] G.Kornaros, Th.Orphanoudakis, H-C.Leligou, *"Architecture and Implementation of Traffic Shaping Integrating Networks-on-Chip and off-chip Networks"*, 2008 International Conference on High Performance Embedded Architectures & Compilers (HiPEAC), 2nd Workshop on Reconfigurable Computing, Göteborg, Sweeden, January 27-29, 2008.

[25] G.Kornaros, D.Meidanis, Y. Papaefstathiou, S.Chantzandroulis, S.Blionas, "Architecture of a Consumer Lab- on-Chip for Pharmacogenomics", IEEE International Conference on Consumer Electronics (ICCE'08), Jan 11-13, 2008, Las Vegas, USA.

[26] *Th.Orphanoudakis, G. Kornaros, I Mavroidis , A.Nikologiannis , I Papaefstathiou: "An Embedded Networking SoC for purely Ethernet MANs/WANs"*, IEEE Symposium on Computers and Communications (ISCC'07), Aveiro, Portugal, July 1-4 2007

[27] G. Kornaros, Y. Papaefstathiou, D. Pnevmatikatos*: "Dynamic Software-Assisted Monitoring of On-Chip Interconnects"*, DATE 2007 Friday Workshop on Diagnostic Services in Network-on-Chips, Palais des Congrès Acropolis Nice, France, Friday April 20, 2007

[28] Ioannis Papaefstathiou, George Kornaros, Nikolaos Chrysos, "*Using Buffered Crossbars for Chip Interconnection*", ACM Great Lakes Symposium on VLSI (GLSVLSI2007), Proceedings of the 17th ACM Great Lakes Symposium on VLSI 2007, Pages: 90 – 95, Stresa-Lago Maggiore, Italy *March 11 - 13, 2007*

[29] George Kornaros, Yannis Papaefstathiou*: "A Buffered Crossbar-Based Chip Interconnection Architecture Supporting Quality of Service"*, SPL2007 - III Southern Conference on Programmable Logic, February 26-28, 2007 - Mar del Plata, Argentina, IEEE Computer Society 2007, ISBN 978-1-4244-0606-7

[30] George Kornaros, "*A Buffered Cross-Bar Switch Fabric Utilizing Shared Memory"*, 9th Euromicro Conference on Digital System Design: Architectures, Methods and Tools (DSD 2006), 30 August - 1 September 2006, Dubrovnik, Croatia, IEEE Computer Society 2006, pp 180-188, ISBN 0-7695-2609-8, http://doi.ieeecomputersociety.org/10.1109/DSD.2006.30

[31] Theofanis Orphanoudakis, Aristides Nikologiannis, Ioannis Papaefstathiou, George Kornaros, Iakovos Mavroidis, Nicholas Zervos: "Custom Network Processor Design for High-Performance Multiservice Access Concentrators". Proceedings of the International Conference IWSSIP 2005 (12th INTERNATIONAL WORKSHOP ON SYSTEMS, SIGNALS & IMAGE PROCESSING), 22-24 September 2005, Chalkida, Greece

[32] Ioannis Papaefstathiou, Theofanis Orphanoudakis, Aristides Nikologiannis, George Kornaros, Iakovos Mavroidis: "Performance Evaluation of a Network Processor Based Multi-Service Access Concentrator". 12th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Gammarth, Tunisia, December 11-14th 2005

[33] Ioannis Papaefstathiou, Theofanis Orphanoudakis, George Kornaros, Christopher Kachris, I. Mavroidis, Aristides Nikologiannis: "Queue Management in Network Processors". (DATE 2005: 112-117) 2005 Design, Automation and Test in Europe Conference and Exposition (DATE 2005), 7-11 March 2005, Munich, Germany. IEEE Computer Society 2005, ISBN 0-7695-2288-2

[34] Ch. Kachris, Th. Orphanoudakis, I. Papaefstathiou, G. Kornaros, A. Nikologiannis, N. Zervos, "Performance Evaluation of Queue Management Implementations in Network Processing Units", WSEAS Transactions on Communications, Issue 1, Volume 4, July 2004, ISSN 1109-2742.

[35] Ioannis Papaefstathiou and George Kornaros, "Software Processing Performance in Network Processors", Design Automation and Test in Europe Conference (DATE'04), 2004 CNIT La Defence Paris, February 16-20, 2004.

[36] Ioannis Papaefstathiou and George Kornaros, "Performance against cost trade-offs for Hardware Compression in 10 Gigabit Networks", 10th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2003), University of Sharjah, Sharjah, United Arab Emirates, December 14-17, 2003.

[37] C.Charopoulos, N.Leligou, G.Stassinopoulos, G.Kornaros, Th.Orphanoudakis, "Programmable peak-rate Gigabit shaper supporting ATM and packet-oriented traffic", International Conference on Computer, Communication and Control Technologies: CCCT '03 and The 9th. International Conference on Information Systems Analysis and Synthesis: ISAS '03, July 31, August 1-2, 2003 - Orlando, Florida, USA.

[38] Th. Orphanoudakis, H.C.Leligou, George Kornaros, Ch. Charopoulos, "Accurate scheduler implementation for shaping flows of variable length packets in high-speed networking applications", *Recent Advances in Communications and Computer Science*, pp. 95-102, 7th WSEAS International Multiconference on Circuits, Systems, Communications and Computers (CSCC 2003) Corfu, Greece, July 7-10, 2003

[39] George Kornaros, Th. Orphanoudakis, N. Zervos, "An Efficient Implementation of Fair Load Balancing over Multi-CPU SOC Architectures", DSD'2003 EUROMICRO Symposium on Digital System Design, Architectures, Methods and Tools, Antalya, Turkey, September 3 – 5, 2003

[40] George Kornaros, Ioannis Papaefstathiou, "An Innovative Resource Management Scheme for Multi-Gigabit Networking Systems", 6th IEEE International Conference on High Speed Networks and Multimedia Communications (HSNMC'03), © Springer-Verlag, Estoril, Portugal, July 23-25, 2003.

[41] I. Papaefstathiou, H.-C. Leligou, Th. Orphanoudakis, G. Kornaros, N. Zervos, G. Konstantoulakis, "An Innovative Scheduling Scheme For High Speed Network Processors", IEEE International Symposium on Circuits and Systems (ISCAS 2003), Bangkok, Thailand, May 25 - 28, 2003.

[42] G. Kornaros, F. Orphanoudakis, I. Papaefstathiou, "Active Flow Identifiers for scalable, QoS scheduling in 10-Gbps network processors", IEEE International Symposium on Circuits and Systems (ISCAS 2003), Bangkok, Thailand, May 25 - 28, 2003.

[43] G. Kornaros, A. Nikologiannis, I. Papaefstathiou, "A Fully-Programmable Memory Management System Supporting Queue Handling at Multi Gigabit rates", IEEE, ACM, 40th Design Automation Conference (DAC), Anaheim, California, U.S.A., June 2-6, 2003.

[44] G.Kornaros, Th. Orphanoudakis, I. Papaefstathiou, "GFS: An Efficient Implementation of Fair Scheduling for multi-Gigabit Packet Networks", IEEE 14th International Conference on Application-specific Systems, Architectures and Processors (ASAP'03), The Hague, The Netherlands, June 24-26, 2003

[45] Theofanis Orphanoudakis, George Kornaros, Ioannis Papaefstathiou, Helen-Catherine Leligou, Stelios Perissakis, Nick Zervos , "Scheduling components for multi-gigabit network SoCs", SPIE's First International Symposium on Microtechnologies for the New Millennium - VLSI Circuits and Systems (EMT102), Maspalomas, Gran Canaria (Canary Islands), Spain, 19 - 21 May 2003.

[46] K.Vlachos, T.Orphanoudakis, N.Nikolaou, G.Kornaros, K.Pramataris, S.Perissakis, J-A.Sanchez, and G.Konstantoulakis, "Processing and scheduling components in an innovative network processor architecture", Proc. of VLSI Design 2003, N.Delhi,India, January 2003.

[47] Georgios Kornaros, Dionisios Pnevmatikatos, Dimitrios Mavroidis, Panagiota Vatsolaki, Georgios Kalokerinos, Chara Xanthaki, Dimitrios Dimitriadis, Dimitrios Serpanos, and Manolis Katevenis : ''*On Optimizing ATLAS I, a 10Gbps ATM Switch",*7th Hellenic Conference on Informatics, August 26-29, 1999, Ioannina, Greece. Selected paper in ''*ADVANCES IN INFORMATICS*" by Dimitrios I. Fotiadis & Stavros D. Nikolopoulos, WorldScientific Press, ISBN 981-02-4192-5, April 2000.

[48] Dionisios Pnevmatikatos, Georgios Kornaros: ''*ATLAS II: Optimizing a 10Gbps Single-Chip ATM Switch",* 12th Annual 1999 IEEE International ASIC/SOC Conference, September 15-18, 1999, Washington, U.S.A.

[49] Georgios Kornaros, Panagiota Vatsolaki, Dionisios Pnevmatikatos, Chara Xanthaki, Georgios Kalokerinos, Dimitrios Serpanos, Manolis Katevenis: ''*Implementation of ATLAS I: a Single-Chip ATM Switch with Backpressure",* Hot Interconnects VI Symposium, August 13-15, 1998, Stanford University, Stanford, California, U.S.A.

[50] Dionisios Pnevmatikatos, Georgios Kornaros, George Kalokerinos, and Chara Xanthaki: ''*The Memory Structures of ATLAS I, a High Performance, 16x16 ATM Switch Supporting Backpressure",* 11th Annual 1998 IEEE International ASIC Conference, September 13-16, 1998, University of Rochester, Rochester, N.Y., U.S.A.

[51] George Kornaros, Christoforos Kozyrakis, Panagiota Vatsolaki, Manolis Katevenis: *'Pipelined Multi-Queue Management in a VLSI ATM Switch Chip with Credit-Based Flow-Control",* 17th Conference on Advanced Research in VLSI, September 15-16, 1997, University of Michigan, Ann Arbor, MI, U.S.A.

[52] P. Vatsolaki, G. Kalokerinos, M. Stratakis , Ch. Xanthaki, M. Ligerakis, G. Kornaros, A. Dollas, G. Papadourakis, M. Katevenis: ''*The Implementation of Telegraphos: a High Speed Communication Architecture",* In Proceedings of the 5th Panhellenic Informatics Conference Athens Greece, December 1995.