Dr. Miltos D. Grammatikakis

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PERSONAL

Greek citizenship. Married, 1 child. Fluent in Greek and English. average in French, German. Primary work-related qualities: diverse background, industry-oriented, innovative ideas, communication and organizational abilities, exploring mind, strong analysis capabilities.

EDUCATION

PhD	Computer Science, May 1991, University of Oklahoma. Dissertation Title: *Packet Routing Algorithms on Generalized Hypercube.*
MS	Computer Science, August 1985, University of Oklahoma.
BS	Physics, June 1983, University of Crete, Greece.

PROFESSIONAL INTERESTS

Operating systems and security. System/network programming. Distributed embedded real-time systems. Automotive diagnostics and security. System- and network-on-chip. System-level design methodology and EDA tools. Multicore programming paradigms. Parallel and distributed systems architecture and programming. Design and performance of communication protocols, routers and interconnects. Design space exploration, especially power dissipation, performance, and reliability. Sequential and parallel discrete-event simulation and validation. Probabilistic modeling and testing. IP modeling.

WORK EXPERIENCE

04/03 −− Professor of Programming Languages in CS Group, General Sciences Dept., and since 2010, Informatics Engineering Dept. *TEI* of Crete, Heraklion, Greece. Deputy Director of AISE Lab on Artificial Intelligence and Systems Engineering, since 2016. Served as CS Chairperson (coordinator, from 09/06 to 08/08) with extensive administation duties, e.g. participation in academic commitees for personnel recruitment at all levels, resource management and postgraduate studies. Tried to organize, plan and harmonize diverse lab activities by understanding and motivating people. Preparation and submission of scientific R&D proposals on different topics. Request for equipment grants and postgraduate student exchanges (Erasmus project with Polytechnic of Ancona, Italy). Liaison with School of Management. Lecturing in BSc and MSc on operating systems, embedded systems, information security, computer simulation, and parallel and distributed systems. Promoting research via nationally/internationally funded projects. External collaborator with *ISD S. A.*, Athens, Greece (2003-2010). Since 2003, continued corporate interaction with *ST Micro* in Grenoble (Advanced Systems Technology Lab and Digital Division). The following major National, European *R&D*, industrial, and open-source projects have been completed.

(1/2015--12/2017) *H2020 TAPPS*.
Helped initiate the proposal and later designed prototype solutions for performance isolation applicable for the smart trolley, a complex system that acts as as hub for monitoring clinical tasks on behalf of the patient, reducing medication errors and integrating vital sign devices, such as the *ST BodyGateway* pulse sensor. Evolved an interest in open automotive security solutions, and experimented with *CAN* bus, engine control unit simulators (*ECUSIM2000*, *ECUSIM5100*), and different types of controllers and sensors via *USB*, *SPI*, and *I2C*.

(10/2013--9/2017) *FP7 – IP DREAMS*.
As principal investigator, designed and implemented an open source, distributed, embedded soft real-time e-Health application for detecting *ECG* arrhythmias in- and out-of-hospital by extending Physionet's *WFDB* software. Implemented Linux and Android drivers for *ST BodyGateway* pulse sensor (a device similar to *Preventice BodyGuardian* Heart supporting 700K patients in *US*), and Linux kernel modules for memory and network bandwidth

regulation for supporting mixed criticality. Evaluated *STNoC* memory interleaving on the same and different memory controllers using the cycle-approximate *gem*5 *STNoC* model, already implemented in *TRESCCA*. *DREAMS* final demonstration involved an in-hospital mixed criticality use-case, combining hard real-time *ECG* analysis with rate-constrained video decoding/streaming. To achieve this, we integrated a complex system with multiple *ST Bodygateway* devices, *Odroid XU*4*s*, a *Xilinx Zynq* FPGA platform integrating *TTTech*'s *TTEthernet* time-triggered flows for *ECG* packets with *STNoC* flows for less critical video traffic over the XtratuM real-time hypervisor, an *ARM Juno* board running two *ARM v*7 virtual machines for *ECG* analysis/visualization and video streaming, and *STM*32*F*4 boards for video rendering. More than 40 key performance indicators (including real-time performance and scalability) were measured on the final platform.

(10/2013--9/2016) *FP*7/*STREP SAVE*.
As workpackage leader, collaborated with *ST Micro* and *Virtual Open Systems* to develop a self-adaptive virtualization-aware high-performance/low-energy heterogeneous system architecture. During this project, designed and modeled (in *SystemC* and *gem*5) hardware-supported job dispatching mechanisms among multicore *CPUs* and *GPUs* (graphics processors) or *DFEs* (dataflow engines) by exploiting concepts related to Heterogeneous System Architecture standard (*HSA*), such as ring buffer, dispatcher/return packet, and doorbell synchronization. A *US* patent application related to low overhead *GPU* job dispatching via a newly proposed architecture has been submitted. *GPU* kernels (*Rodinia* benchmarks) were run on the *Mali GPU* of an *Odroid XU*3 in order to measure current dispatch overheads (e.g. miss ratios, delays).

(10/2012--9/2015) *FP*7/*STREP TRESCCA*.
As principal investigator, collaborated with *ST Micro* on the design, modeling, and prototype implementation at the network interface on Zedboard FPGA of an on-chip hardware firewall, including Linux system driver. The firewall targets memory protection against logical on-chip attacks (virus, corrupt devices). System models were developed on top of a cycle-approximate *gem*5 model of the *STNoC* backbone, designed and implemented also during this project. The final demonstration focused on protecting the driver of the *ST BodyGateway* pulse sensor, and included graphical visualization of the attack vectors using security event correlation, heatmaps, and flamegraphs. A *US* patent application related to security and virtualization had been submitted and accepted. In addition, using collateral funds, an off-chip firewall consisting of a Linux kernel module, with a supportive user-space framework for conflict resolution was recently implemented, cf. *https*://*sourceforge*.*net*/*projects*/*netfirecore*.

(6/2012--12/2015) *FP*7/*STREP ASHSHMEM*.
As principal investigator, collaborated with *NTUA*, Athens and *UNIVPM*, Ancona, Italy on automated design of efficient hierarchical shared memory systems for scientific and distributed database applications, with emphasis on hardware support for *DMAs*, load balancing, broadcast, and scatter/gather operations at the level of the memory controller. A *SystemC* model library, including models of routers, on-chip networks, *CPUs* and memory components was delivered as open source software, cf. *https*://*sourceforge*.*net*/*projects*/*hsoc*.

(10/2010--1/2014) *FP*7/*STREP VIRTICAL*.
As task leader, collaborated with *ST Micro*, *Virtual Open Systems* on developing a prototype hardware *IOMMU* module which provides portability with, and extends existing *ARM v*7*a SMMU* (system memory management unit) architecture with virtualization support for heterogeneous multicore SoC. The design was modeled in cycle-accurate, bit-accurate *SystemC* and was validated with actual memory allocation requests, using values of the *MMU* registers and *RAM* memory descriptor files obtained from *ARM FastModels* in bare metal, and from pagemap analysis programs run under Linux. An *IOMMU* prototype was synthesized on *ARM Versatile Express* platform *FPGA* and it's operation was demonstrated using bare metal system drivers.

(4/2010--4/2013) *ENIAC*/*JU SMART*.
As external collaborator with *ISD*, worked with *ASTUS S*. *A*. and *Numonyx* to design secure nonvolatile memories for smart cards, *USB* sticks and other embedded devices. Our design is based on the new standard *AES* block cipher with a fixed block size of 128 bits (*Rinjdael*) and provides confidentiality, data integrity and authentication modes of operation. The current *RTL* model has a complexity of 30K GE, provides 240Mb/sec bandwidth (encryption/decryption) in 32nm *CMOS* process technology with only 3 levels and uses a clock period 4.5ns. *SystemC* models of the system were developed prior to implementation and security of our implementation (intrusiveness) was checked by *Thales e − security*.

(3/2009--3/2011) *ENIAC MODERN*.
As principal investigator managed *ISD*'s technical contribution related to the initiation and development of *MODERN*. Examined fundamental high-level concepts and methodologies for supporting sustained performance and power-efficiency in unreliable SoC and NoC designs. More specifically, focusing on NoC faults, fault diagnosis, as well as fault tolerant routing and dynamic reconfiguration schemes based on m-out-of-n encoding, redundant data allocation and innovative lattice topologies that provide simple, on-the-fly allocation of redundant programmable routers through additional data paths are developed. Energy-aware multicore SoC design through distributed dynamic power management of power-manageable components (*PMC*), such as processor cores and memories, is also explored at system-level. In addition, analog mixed signal blocks, such as phase-locked loop, low noise amplifiers and AD converters, have been simulated using *OSCI*'s *SystemC − AMS* 1.0 standard to examine faul tolerance issues due to aging effects. In this case, by using a set of redundant components. a digital controller can use selected parameter metrics to perform built-in test, detect and repair process from a set of redundant, standby components.

(1/2009--3/2011) *Artemis SCALOPES*.
As principal investigator managed *ISD*'s technical contribution to the initiation and development of *SCALOPES*. Implemented and evaluated power-efficient hybrid programming models (supporting simultaneous message passing, shared memory and streaming or transactional-memory paradigms) for executing multimedia applications on multicore systems-on-chip. Moreover, important problems, such as protocol deadlock, are examined from a low-cost, high performance algorithmic perspective.

(2004--2010) *ST Microelectronics Spidergon STNoC* Industrial Project.
As external collaborator with *ST Microelectronics*, participated in architecture design and modeling of a commercial packet-switched network-on-chip (called *Spidergon STNoC*) aiming at future multiprocessor system-on-chip architectures using *OCCN* and *SystemC* (*IEEE* 1666) framework. To support NoC selection at system-level, an array of open tools for evaluating and analyzing graph theoretical metrics (*Nauty*), generating application task graphs (*TGFF*) and performing application mapping (*Metis*, and *Scotch*), visualization (*Dotty*, *Neato*, and *VCD*) and efficient simulation (*OmNet++*) have led to a Linux-based customized NoC design toolsuite: *Iput*, *Imap*, *Irun*, and *Isee*. *Spidergon STNoC* is featured in tens of publications, hundreds of industrial web pages, and articles of popular international electronic design magazines, such as EE Times, New Electronics and Embedded Systems Journal. Derivative *Spidergon STNoC* FPGA designs with *ARM* processors and *DDR* controllers are succesfully commercialized by *ST Microelectronics*. Since 2008, proprietary work with *ST Microelectronics* concentrated on 2-d and 3-d hierarchical *Spidergon STNoC* architecture extensions and global system solutions.

(2006--2008) *IST*/*PULLNANO* Project.
As principal investigator, managed *ISD*'s technical contribution to initiation and development of *IST*/*PULLNANO*. Focused on designing and validating bit- and cycle-accurate *SystemC* transaction-level models of an Ethernet network bridge and a multicast router integrated in a 64-node on-chip network supporting *SIMD* array processing macro-operations common in multimedia applications. These simulation models have focused on system-level design space exploration, for system-level estimation, analysis and management of dynamic power

consumption. Relative power estimation has been based on counting transactions and/or bit-transitions, while calibration models have also been developed. Models have been used as computation-, communication- and memory-bound benchmark applications for future deep submicron CMOS technology roadmaps. The proposed power estimation approach can be extended for early analysis and power optimization of any soft, firm or hard IP implemented in current technology. This idea can be further extended to future technology generations by introducing tools, such as MASTAR (or GTX) that can annotate simulated CMOS roadmap values for future 22/32nm technology nodes and variations directly into high-level cycle- and bit-accurate SystemC-based models, thus providing technology-related speed, power dissipation and variability parameters.

(2003--) Open Source Project: On-Chip Communication Network (*OCCN*).
Established, managed, contributed and maintained (as team leader and key participant) the only available open-source network-on-chip (*NoC*) modeling and design exploration framework via *http://occn.sourceforge.net*. *OCCN* was based on the *SystemC*-based design library and simulation kernel, and provided user/developer methodology focusing on plug-and-play communication refinement, on-chip communication channel design examples (bus, point-to-point, and multiaccess), and advanced visualization features with analysis capabilities. *OCCN* target platforms were Solaris 2.8 and Linux (Redhat). *OCCN* has been heavily cited and utilized by over 600 organizations worldwide (with more than 2400 recorded downloads), including prestigious Academic Schools, research institutes and semiconductor, electronics and EDA industry. *OCCN* received the *ST* Corporate Community of Practice Gold Trophy Award in 2005, and was referenced in the 2005 edition of the EDA Roadmap. *OCCN* has been converted to work with *SystemC* 2.2 and *gcc*4+ compilers, while more features, such as application modeling, code generation and automated testing, will be added in the future.

10/00 −− 04/03 Senior Software Engineer, *ISD S.A.*, Athens, Greece. Technical director at *ISD*, Heraklion Branch (2000--2002). Technically, he worked on SoC design languages and models in close collaboration with *ST Microelectronics*, *AST* Grenoble Research Lab.

(2000--2003) *IPSim* Design Environment for System-Level IP/SoC Modeling.
Jointly with *ST Microelectronics - AST − Grenoble* contributed (as one of the primary architects) to the documentation, design, development, validation, optimization (through redesigning and customizing existing debuggers and profilers) and technical support of the *IPSim* design language methodology, custom system-on-chip (SoC) modeling library, simulation kernel, and runtime environment for system-on-chip design. The *IPSim* library contained 1000+ user-level functions for objects, such as fixed data types, processes, hierarchical finite state machines, different kinds of FIFOs and memory, cache (unified, data and instruction cache), intra- and inter-module communication and synchronization objects (including complex, hybrid models for *Mailbox*, *Message Box*), bus, point-to-point or multiaccess communication channels, and automated high-level performance modeling and visualization; *IPSim* target platforms were Solaris 2.5.1 through Solaris 8. *IPSim* enabled the design of complex on-chip communication networks, such as the *ST Microelectronics STBus*, a real product found today in almost any digital satellite decoder. *IPSim* was extensively tested through the BroadBand Network Terminator (*BBNT*) SoC, a fairly complex gateway (over 100K *IPSim* lines of code) proposed to Cisco Systems Inc. Part of the *IPSim* library has been ported to the *Synopsys Cocentric Studio* for internal *ST Microelectronics* system-level design and IP integration (plug-in available on the market since 2003).

(2001--2003) *MEDEA+ ToolIP* Project (Tools for IP).
As principal investigator, managed *ISD*'s technical contribution to initiation and development of *Medea+ project ToolIP*, "*Tools* and *Methods* for *IP Reuse*". *ToolIP* addressed the complexity of current SoC design by using system-level modeling and verification techniques, applying design reuse with qualified and parametric IP cores, and providing a seamless design flow integrating existing and emerging tools. *IPSim* development has been partially supported through this project, while certain library objects for intra-module

communication and synchronization (especially interface methods) have been proposed to industry standardization initiatives (initially *OSCI SystemC*, and later *IEEE* 1666) and are now part of the SystemC design language.

09/02 to 08/05 Visiting Associate Professor, Dept. Material Science and Technology, University of Crete. Lecturing on "Computer Programming" (F77, and partly F90 or HPF) and "Numerical Analysis".

01/00 to 06/00 - 09/02 to 04/03
Part-time lecturing on "Algorithms and Data Structures". Full-time lecturing on "Introduction to Computer Science" courses at *TEI* of Crete.

07/99 to 09/00 Software Engineer, Development Programmes, Intracom, Peania, Greece. Developed a multi-layered distributed performance simulation and visualization tool for *ATM* networks (initially supported by Ericsson). Examined new middleware services supporting distributed application monitoring, load balancing and reconfiguration, by focusing on automatic static and dynamic task allocation facilities (*Eurescom project − P*924). Performed validation and *QoS* assessment on the virtual private network of the *EuroSkyWay* satellite network (*EU TEN Trans − European Network Project REVENUES*). This involved simulation, traffic classification (e.g. email, ftp, http) and applying self-similarity.

01/99 to 07/99 Scientific Assistant (C1), transferred to: University of Oldenburg, Germany.

07/95 to 12/98 Scientific Assistant (C1), Institute of Informatics, University of Hildesheim, Germany. Taught senior year courses on supercomputing, parallel programming and interconnection networks, and seminars on simulation and modeling. Supervised MS thesis and student seminar work. Administered the Institute webpages. Worked together with students on developing a discrete-event, cycle-level *ATM* switch and cell-level network simulators. All simulators were run on massively parallel systems (Cray T3D/T3E, TMC CM-5) and networks of workstations, using shared memory, message passing and data parallel programming models. Participated in *EU ESPRIT* WG *Simulation in Europe (SiE)*, *EU TMR TRACS* and *German DAAD* short-term exchange projects. Was granted and used over 6K hours of supercomputing time at KFA/Juelich, CNCPST/Paris and EPCC/Edinburgh for research purposes.

07/92 to 06/95 Research Associate, Architecture & VLSI group, *ICS FO.R.T.H.*, Crete, Greece. Within *EU ESPRIT R&D* project *SHIPS* (Supercomputer Highly Parallel System) worked on system-level simulation (in *C* language), hardware verification, and performance modeling of a prototype communication switch (*Telegraphos I*) and processor to/from network interfaces for interconnecting *DEC* A workstations into a distributed system. Lectured part-time at *TEI* of Crete in Heraklion, Greece.

06/91 to 06/92 Postdoctoral Fellow, Laboratoire de l' Informatique du Parallelisme, Ecole Normale Superieure de Lyon. Helped in developing a research proposal on Communication Complexity. Was involved in an implementation of dictionary machines on a *MasParMPI* 1024-node parallel architecture. Provided student seminars on multiprocessor communication and fault tolerance issues. Participated in the French working group on communication algorithms and interconnection networks. Committed to developing research proposals.

08/88 to 05/91 Teaching Assistant, Dept. of Computer Science, University of Oklahoma. Responsible for introductory programming courses (*FORTRAN* and *PASCAL*), operating system, data structures, and computer architecture courses.

Summer 88-89 Research Assistant, Dept. of Computer Science, University of Oklahoma. Designed, coded and tested software for *CAD*-specific applications, i.e. 2d Voronoi diagram, splay trees.

12/85 to 09/87 Researcher, Greek Army. Partly involved in automated battlefield information acquisition and communication exploitation systems (*BICES*).

08/85 to 12/85 Maintenance programmer and statistical analyst, Dept. of Education, University of Crete. Data mining and statistical analysis of large databases involving Higher Education (Greek University and *TEI*) entrance examinations.

08/84 to 05/85 Grading Assistant, Dept. of Computer Science, University of Oklahoma.

BOOKS

[1] M.D. Grammatikakis, M. Coppola, R. Locatelli, G. Maruccia, L. Pieralisi, "Interconnect Processing Units: Spidergon STNoC", CRC press, September 2008, ISBN: 978-1-4200-4471-3, 288 pages. Book foreword written by Prof. William J. Dally, Chairman of Computer Science, Stanford University.

[2] M.D. Grammatikakis, D. F. Hsu and M. Kraetzl, "Parallel System Interconnections and Communications", CRC press, December 2000, ISBN: 0-849-33153-6, 412 pages. Received "Editor's choice award" in IEEE Network column "New Books and Multimedia", July 2001.

PATENTS

[1] M. Coppola, G. Kornaros, and M.D. Grammatikakis, "Apparatus and methods implementing dispatch mechanisms for offloading executable functions", *US Patent, 20170206169 A1*, 2017

[2] M. Coppola, G. Kornaros, and M.D. Grammatikakis, "Resource access control in a system-on-chip", *US Patent, 9519596 B2*, 2015.

EDITED BOOKS

[1] M.D. Grammatikakis, G. Kornaros and N. Papadakis (Eds.), *in Proc. 8th Workshop on Intelligent Solutions in Embedded Systems (WISES2010)*, Heraklion, Greece, 2010. IEEE Catalog No: CFP10848-PRT/ART.

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[5] M.D. Grammatikakis, A. Papagrigoriou, P. Petrakis, and M. Coppola, "System-level modeling and SystemC", (invited chapter), in *EDA for Integrated Circuits Handbook Handbook*, Eds. M. Grant, L. Lavagno and I. Markov, Taylor & Francis Group, CRC Press, Chapter 12 (30 pages), 2016.

[6] M.D. Grammatikakis, G. Kornarosm and M. Coppola, "Power-aware multicore SoC and NoC design", (invited chapter), in *Multiprocessor System-on-Chip: Current Trends and Future*, Eds. M. Huebner and J. Becker, Chapter 8, Springer Verlag, ISBN:978-1-4419-6459-5, 29 pages, 2011.

[7] L. Bononi, N. Concer, and M. Grammatikakis, "System-level tools for NoC-based multicore design" in *Embedded Multicore Architectures*. Ed. G. Kornaros, Chapter 6, CRC Press, Taylor and Francis Group, 40 pages, 2009, accepted.

[8] M.D. Grammatikakis, M. Coppola, T. Basset, C. Grassman, and P. Kajfasz, "IP reuse", (invited chapter), *The Medea+ Design Automation Roadmap*, Eds. J. Borel, Chapter 9, 18 pages, (initially) 2005, ISBN: 2-9520704-2-3. Updated in 2008, as Chapter 7, 40 pages.

[9] M.D. Grammatikakis and M. Coppola, "Cycle-accurate system-level modeling and performance evaluation", (invited chapter), in *Electronic Design Automation for Integrated Circuits Handbook*, Eds. G. Martin, L. Lavagno and L. Scheffer, Chapter 11, Taylor and Francis Group, CRC Press, 34 pages, 2005, ISBN: 0-8493-3096-3.

[10] M.D. Grammatikakis, M. Coppola, R. Locatelli, G. Marrucia, and L. Pieralisi, "Spidergon: a NoC modeling paradigm", (invited chapter), in *Model Driven Engineering for Distributed, Real-Time, and Embedded Systems*, Eds. S. Gerard, J.-P. Babau, and J. Champeau, Hermes Publisher, Chapter 13, 19 pages, 2005, ISBN: 9781905209323.

[11] M.D. Grammatikakis, M. Coppola, and F. Sensini, "Software for multiprocessor networks on chip", (invited chapter), *Networks on Chip*, Eds. A. Jantsch and H. Tenhunen, Kluwer Academic Publisher, 24 pages, 2003, ISBN: 1-4020-7392-5. This book has made record sales for Kluwer, outselling the recent SystemC book.

[12] M.D. Grammatikakis, M. Kraetzl, and E. Fleury, "Shortest-path and hot-potato routing on unbuffered toroidal networks", (invited chapter), *Defense Applications of Signal Processing*, Eds. W. Moran, D. Cochran and L. B. White, Elsevier (North Holland), 2001, ISBN: 0-444-50864-3.

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[1] M.D. Grammatikakis, K. Papadimitriou, P. Petrakis, A. Papagrigoriou, G. Kornaros, I. Christoforakis, O. Tomoutzoglou, G. Tsamis, and M. Coppola, "Security in MPSoCs: a NoC firewall and an evaluation framework", *IEEE Transactions on TCAD,* **99**, 2015, pp. 1344-1357.

[2] M.D. Grammatikakis, M. Coppola, S. Curaba, R. Locatelli, G. Marrucia, and F. Papariello, "OCCN: A NoC modeling framework for design exploration", *J. Syst. Arch. - Special Issue on Network-on-Chip* , Elsevier (North Holland), **50 (2-3)**, 2004, pp. 129--163.

[3] M.D. Grammatikakis and S. Liesche, "Priority queues and sorting methods for parallel simulation", *IEEE Trans. Software Engin. - Special Section on Arch. Independent Lang. and Software Tools for Parallel Proc.*, **SE-26 (5)** , 2000, pp. 401--422.

[4] M.D. Grammatikakis, D. F. Hsu, M. Kraetzl and J. Sibeyn, "Packet routing in fixed-connection networks: a survey", *J. Parallel Distrib. Comput.*, Academic Press, **54** , 1998, pp. 77--132.

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[6] M.D. Grammatikakis, F. K. Hwang and Y. C. Yao, "D-move local permutation routing for the d-cube", *Discrete Appl. Math.*, Elsevier (North Holland), **72 (3)** , 1997, pp. 199--207.

[7] M.D. Grammatikakis and A. G. Ferreira, "Randomized routing on generalized hypercubes", *Theoret. Comput. Sci.*, Elsevier (North Holland), **158 (1-2)** , 1996, pp. 53--64.

[8] M.D. Grammatikakis, (one section in) "Open problems in interconnection networks", *Parallel Proc. Letters - Special Issue on Algorithmic and Structural Aspects of Interconnection Networks*, eds. P. Fraigniaud, A. Liestman, D. Sotteau, World Scientific Publishing, **4** , 1993.

PUBLICATIONS IN CONFERENCE PROCEEDINGS

[1] G. Tsamis, M.D. Grammatikakis, A. Papagrigoriou, P. Petrakis, V. Piperaki, A. Mouzakitis and M. Coppola, "Soft real-time smartphone ECG processing", *in Proc. 12th IEEE International Symposium on Industrial Embedded Systems*, 2017.

[2] M.D. Grammatikakis, G. Tsamis, P. Petrakis, A. Mouzakitis, M. Coppola, "Network and memory bandwidth regulation in a soft real-time healthcare application", *in Proc. 13th Workshop on Operating Systems Platforms for Embedded Real-Time Applications*, 2017.

[3] A. Papagrigoriou, P. Petrakis, M.D. Grammatikakis, "A firewall module resolving rules consistency". *in Workshop on Intelligent Embedded Systems", 2017.*

[4] P. Petrakis, M. Abuteir, M.D. Grammatikakis, K. Papadimitriou, R. Obermaisser, Z. Owda, A. Papagrigoriou, M. Soulie, M. Coppola, "On-Chip Networks for mixed-criticality systems", *in Proc. IEEE Int. Conf. Application-Specific Systems, Architectures and Processors (ASAP)*, London, UK, 2016.

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[8] M.D. Grammatikakis, A. Papagrigoriou, P. Petrakis, K. Harteros, and G. Kornaros, "Load balancing, broadcast, and scatter primitives for efficient multicore applications", *in Workshop on Intelligent Embedded Systems", 2015.*

[9] K. Papadimitriou, P. Petrakis, M.D. Grammatikakis and M. Coppola, "Security enhancements for building saturation-free, low-power NoC-based MPSoCs", *in Proc. IEEE Conference on Communications and Network Security (CNS) - 1st IEEE Workshop on Security and Privacy in Cybermatics*, 2015.

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[12] G. Schomaker, A. Herrholz, G. Duc, R. Pacalet, S. Raho, M. Grammatikakis, M. Coppola, I. Garcia Vega, "Trustworthy embedded systems for secure cloud computing", *in Proc. 8th Int. Conf. Availability, Reliability and Security (ARES)*, 2013.

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[14] M.D. Grammatikakis, A. Papagrigoriou, P. Petrakis and G.Kornaros, "Monitoring-aware virtual platform prototype of heterogeneous NoC-based multicore SoCs", *in Proc. 16th Euromicro DSD*, 2013.

[15] M.D. Grammatikakis, A. Papagrigoriou, P. Petrakis and G. Kornaros, "Non-intrusive NoC DFS for soft real-time multimedia applications", *in Proc. 16th Euromicro DSD*, 2013.

[16] G. Kornaros, K. Harteros, M. Astrinaki, I. Christoforakis, M. Coppola, and M D. Grammatikakis, "An IOMMU for hardware-assisted full virtualization of heterogeneous multicore SoCs", *in Proc. Int. Conf. VLSI Circuits and Systems VI*, SPIE Microtechnologies, 2013.

[17] G. Kornaros, M.D. Grammatikakis, and M. Coppola, "Towards full virtualization of heterogeneous NoC-based multicore embedded architectures", *in Proc. 10th IEEE/IFIP Int. Conf. Embedded and Ubiquitous Computing (EUC)*, 2012.

[18] M.D. Grammatikakis, S. Politis, J.-P. Schoellkopf and C. Papadas. "System-level power estimation methodology using cycle- and bit-accurate TLM", *in Proc.* 14*th Design Automation and Test in Europe*, 2011.

[19] M.D. Grammatikakis, L. Bononi, N. Concer, M. Coppola, R. Locatelli, "NoC topologies exploration based on mapping and simulation models", *in Proc. Digital Systems Design Conf. (DSD)*, 2006, pp. 546--549.

[20] M.D. Grammatikakis, M. Coppola, S. Curaba, G. Marrucia, and F. Papariello, "OCCN: A network-on-chip modeling and simulation framework", *in Proc.* 7*th Design Automation and Test in Europe*, 2004, Paris, France, Vol. 3, pp. 174-179.

[21] M.D. Grammatikakis, M. Coppola, S. Curaba and G. Marrucia, "IPSIM - SystemC 3.0 enhancements for communication refinement", *in Proc.* 6*th Design Automation and Test in Europe*, 2003, Munich, Germany, Vol. 2, pp. 106--111.

[22] M.D. Grammatikakis and T. Merker, "Consistency models and synchronization on *Cray-T3E*", *in Proc.* 5*th SGI/Cray MPP Workshop*, Bologna, Italy, 1999, pp. 248--257. Available from http://www.cineca.it/mpp-workshop/proceedings.htm

[23] M.D. Grammatikakis, N. Fideropoulos, F. Howell, S. Liesche, T. Thielke and A. Zachos, "Network simulation on CM5 by sorting integer conflict functions", *in Proc. Parallel Comput. Conf. (PARCO)*, Bonn, Germany. Advances in Parallel Comput., Vol. 12, Elsevier (North Holland), 1998, pp. 459-462.

[24] M.D. Grammatikakis and S. Liesche, "Parallel priority queues on *Cray-T3E*", *in Proc.* 4*th SGI/Cray MPP Workshop*, Munich, Germany, 1998, pp. 69--91. Available from http://www.rzg.mpg.de/mpp-workshop/papers/ipp-report.html

[25] M.D. Grammatikakis, H. Dollani and S. Liesche, "Synchronization on *Cray-T3E* virtual shared memory", *in Proc.* 4*th SGI/Cray MPP Workshop*, Munich, Germany, 1998, pp. 50--58. Available from http://www.rzg.mpg.de/mpp-workshop/papers/ipp-report.html

[26] M.D. Grammatikakis, H. Dollani and M. Kraetzl, "Continuous multicasting on statically-allocated VC-based switches", *IEEE Conf. Global Comm. (GLOBECOM)*, Sydney, Australia, 1998, pp. 2387--2392.

[27] M.D. Grammatikakis, C. Eilers, M. Kraetzl, S. Liesche and T. Thielke. "Data parallel communication and sorting on CM5", *in Proc. 5th Australasian Conf. Parallel Real-Time Syst. (PART'98)*, Adelaide,

Australia. Springer Verlag, 1998, pp. 132--140.

[28] M.D. Grammatikakis, H. Dollani and S. Liesche, "Synchronization on *Cray-T3E* virtual shared memory", *in Proc.* 40th *Cray Users Group Conf.*, Stuttgart, Germany, 1998. Preliminary version of [4] (above).

[29] M.D. Grammatikakis, N. Fideropoulos and A. Zachos, "Network simulation on *Cray-T3E* using MPI", *in Proc.* 3rd *SGI/Cray MPP Workshop*, Paris, France, 1997. Available from http://armoise.saclay.cea.fr/~workshop/Program.html

[30] M.D. Grammatikakis, M. Kraetzl and E. Fleury, "Shortest-path and hot-potato routing on unbuffered 2-d tori", *IEEE Conf. Global Comm. (GLOBECOM)*, Phoenix, AZ, 1997, pp. 165--169.

[31] M.D. Grammatikakis, M. Kraetzl and E. Fleury, "Shortest-path and hot-potato routing on unbuffered toroidal networks", *AFOSR Workshop Defense Signal Proc.*, Victor Harbor, South Australia, 1997 (invited paper).

[32] M.D. Grammatikakis, A. G. Ferreira and E. Fleury, "Multicasting control and communications on multihop stack-ring OPS networks", *in Proc.* 4th *IEEE Conf. Massively Parallel Proc. using Optical Interconnections (MPPOI)*, Toronto, Canada, 1997, pp. 39--44.

[33] M.D. Grammatikakis and M. Johl, "Clock level simulations of an ATM Switch", *in Proc. SCS Euro Media Conf.*, London, UK, 1996, pp. 149--156.

[34] M.D. Grammatikakis, "Parallel simulation of ATM switches and networks", *in Proc.* 2nd *SGI/Cray MPP Workshop*, Edinburgh, Scotland, UK, 1996. Available as http://www.epcc.ed.ac.uk/t3d/workshop/proceedings/Grammatikakis.ps.gz.

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[36] M.D. Grammatikakis, D. F. Hsu and M. Kraetzl, "A journey into multicomputer routing algorithms", Keynote Paper, *in Proc.* 1st *IEEE Symp. Parallel Alg. Arch. Synth. (PAS)*, Aizu, Japan, 1995, pp. 19--27. Keynote paper for PAS Conference.

[37] M.D. Grammatikakis and M. Kraetzl, "Probabilistic models of network routers", *in Proc. Parallel Computer Conf. (PARCO)*, Ghent, Belgium. Advances in Parallel Comput., Vol. 11, Elsevier (North-Holland), 1995, pp. 613--616.

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[43] M.D. Grammatikakis, J. S. Jwo and A. Damianakis, "Simulating communication in parallel computer systems", *in Proc. SCS Eur. Sim. Symp. (ESS)*, Delft, The Netherlands, 1993, pp. 477--482.

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[46] M.D. Grammatikakis and J. S. Jwo, "Greedy permutation routing on cayley graphs", *in Proc.* 2nd *Joint Int. Conf. Vector and Parallel Proc. (CONPAR)*, Lyon, France. Lecture Notes in Computer Science, Springer Verlag, Vol. 634, 1992, pp. 839--840.

[47] M.D. Grammatikakis and J. S. Jwo, "A discrete-event simulator of communication algorithms in interconnection networks", *in Proc.* 9th *Symp. Theor. Aspects Comput. Sci. (STACS)*, Paris, France. Lecture Notes in Computer Science, Springer Verlag, Vol. 577, 1992, pp. 609--610.

[48] M.D. Grammatikakis, "Probabilistic routing algorithms for generalized hypercubes", *in Proc.* 25th *Conf. Inf. Sci. Syst. (CISS)*, Baltimore, MD, 1991, pp. 125--131.

[49] M.D. Grammatikakis, "Probabilistic routing in distributed architectures", *in Proc.* 5th *SIAM Conf. Parallel Proc.*, Houston, TX, 1991, (abstract).

[50] M.D. Grammatikakis, S. Lakshmivarahan and S. K. Dhall, "Packet routing for generalized hypercube", *in Proc.* 24th *Conf. Inf. Sci. Syst. (CISS)*, Princeton, NJ, 1990, pp. 159--164.

[51] M.D. Grammatikakis, S. Lakshmivarahan and S. K. Dhall, "Experiments on probabilistic routing for a generalized hypercube", *in Proc.* 3rd *Symp. Applied Comput. (SAC)*, Stillwater, OK, 1989, pp. 131 - 133.

OTHER PRESENTATIONS IN WORKSHOPS

[1] M. Grammatikakis, M. Coppola and R. Locatelli, "STNoC services modeled in gem5 for High Performance MPSoC", *Nanoelectronics, Applications, Design & Technology Conference*, 2016.

[2] M. Grammatikakis, G. Kornaros, K. Papadimitriou, Y. Christoforakis, P. Petrakis and A. Papagrigoriou, "Load balancing, broadcast, scatter primitives for efficient nulticore applications", (poster presentation), *HIPEAC*, 2016

[3] M. Grammatikakis, G. Kornaros, K. Papadimitriou, Y. Christoforakis, P. Petrakis and A. Papagrigoriou, "System-level modeling of a NoC firewall on Spidergon STNoC", (invited presentation), *EU Cyber Security and Privacy Forum Conf.*, 2014

[4] M.D. Grammatikakis, M. Coppola, S. Curaba, G. Marrucia, and F. Papariello, "OCCN: A NoC modeling framework for design space exploration", European SystemC Users Group Meeting, Stuttgart, Germany, November 2003.

[5] M.D. Grammatikakis, M. Coppola, S. Curaba, G. Marrucia, and F. Papariello, Project Results A511 - TOOLIP", Berlin, Germany, November 2003.

[6] M.D. Grammatikakis, M. Coppola, S. Curaba, G. Marrucia, and F. Papariello, "OCCN: A NoC modeling framework for design exploration", (invited presentation), *Int. Forum of Specification and Design Languages* , Frankfurt, Germany, September 2003.

[7] M.D. Grammatikakis, M. Coppola, S. Curaba, G. Marrucia, and F. Papariello, "OCCN: An environment for NoC exploration", 3rd *Int. Seminar on Application-Specific Multi-Processor SoC* , Chamonix, France, July 2003.

[8] M.D. Grammatikakis, M. Conti and M. Coppola, "IPSIM - SystemC2.0", 2nd *Workshop, EU Medea+ Project TOOLIP (A511)*, Madrid, Spain, January 2002. Paper appeared in Medea+ Conf. Proceedings, 2002, pp. 3--12.

[9] M.D. Grammatikakis and M. Coppola, "ToolIP: a step towards SoC design", (invited presentation), *Medea+ conference*, Veldhoven, Holland, October 2001.

[10] M.D. Grammatikakis, "Towards an automatic task assignment tool", *Eurescom* meeting - *P924*, Athens, Greece, September 2000.

[11] M.D. Grammatikakis, "Specifications of middleware monitoring service supporting application reconfiguration", *Eurescom* meeting - *P924*, Athens, Greece, September 2000.

[12] M.D. Grammatikakis, "VPN service of the *EuroSkyWay* satellite network", *EU TEN/TELECOM* project - *REVENUES*, project review, Brussels, Belgium, May 2000.

[13] M.D. Grammatikakis and S. Liesche, "Parallel priority queues on *Cray-T3E*", *EU TMR TRACS Users Group Meeting*, EPCC, Edinburgh, Scotland, September 1998.

[14] M.D. Grammatikakis, M. Kraetzl and E. Fleury, "Shortest-path and hot-potato routing on unbuffered 2-d tori", *Int. Workshop on Interconnection Networks*, Prague, Czech Republic, July 1997.

[15] M.D. Grammatikakis, "Viewpoints at communication protocol development", *Workshop on Parallel Environments with Petri-nets (PEP)*, Hildesheim, Germany, May 1996.

[16] M.D. Grammatikakis, "Models of network routers", *Int. Workshop on Interconnection Networks*, Lumigny, France, July 1995.

[17] M.D. Grammatikakis, "Optimal *d*-cube routing, complexity of combining networks", *Int. Workshop on Interconnection Networks*, Lumigny, France, July 1993.

[18] M.D. Grammatikakis, "Routing on generalized hypercube", *Int. Workshop on Interconnection Networks*, Lumigny, France, August 1991.

RECENT TRAINING VISITS

[1] Numerous weekly visits to *ST Microelectronics* (*AST Lab*) in Grenoble, France, 2000--. Heavily involved in team discussions concerning roadmap, requirement analysis, demonstrations, presentations, and operational (design and code) reviews.

[2] Participation in operational reviews of several industrial IT projects and/or demonstrations with the *European Space Agency*, Athens, Greece, October 2008.

[3] Participation in operational reviews of several industrial IT projects at *Alenia Aeronautica*, Torino, Italy, 2005-2006.

[4] Invitation for short visit to *Telecom Italia* (TILAB), L' Acquila, Italy, 2002 and 2003.

[5] Short training visit and workshop on "Standardization of SystemC-based bus models" at *Synopsys Inc*., Paris-Rungis, France, March 2002.

[6] Short training visit and seminar on "*Synopsys Cocentric Studio*" at *Synopsys Inc*., Leda Lab, Grenoble, France, November 2001.

[7] Training visit and Eurescom workshop on "Dynamic reconfiguration of distributed CORBA-based systems", *GMD Focus* Lab, Berlin, Germany, July 2000.

[8] Extended research visit to Edinburgh Parallel Computing Centre (*EPCC*), Scotland, July & August 1996.

[9] Short research visits to Ecole Normale Superieure de Lyon/LiP in Lyon, France, Paderborn Center for Parallel Computing in Paderborn, Germany, IMEC-VSDM in Leuven, Belgium, and Max Planck Institute for Informatics in Saarbruecken, Germany, 1995-1998.

MS THESIS SUPERVISION

[1] Paraskevi Piperaki (currently with *TEI* of Crete), "Security primitives in a hierarchical GNU/Linux driver of a hardware NoC firewall", MS Thesis, *TEI* of Crete, Greece, June 2016.

[2] Torsten Merker (currently with Hewlett-Packard), "Consistency models and synchronization on *Cray-T3E* virtual shared memory", Diploma (MS) Thesis, University of Oldenburg, Germany, June 1999.

[3] Stefan Liesche (currently with IBM), "MPI and shared memory implementations of priority queues for parallel simulation on *Cray-T3E*", Diploma (MS) Thesis, University of Hildesheim, Germany, May 1998.

[4] Martina Johl (currently with University of Frankfurt), "Performance experiments with a realistic ATM router", Diploma (MS) Thesis, University of Hildesheim, Germany, March 1997.

INTERNAL MANUSCRIPTS (EXCLUDES SEVERAL EU PROJECT DELIVERABLES)

[1] M.D. Grammatikakis, M. Coppola, R. Locatelli, L. Pieralisi, and G. Maruccia, "Theoretical metrics and mapping heuristics for NoC topology selection: a case study on Spidergon STNoC", 25 pages, internal report, AST Grenoble Lab, Grenoble, France, 2006.

[2] M.D. Grammatikakis, M. Coppola, R. Locatelli, L. Pieralisi, and G. Maruccia, "The Spidergon NoC interconnect: white paper", 54 pages, internal report, AST Grenoble Lab, Grenoble, France, 2005. Several *ST Microelectronics* corporate electronic magazine articles on Spidergon STNoC were actually

based on open (non confidential) parts of this report.

[3] M.D. Grammatikakis, and M. Coppola, "Advanced SoC modeling based on SystemC 2.0", 75 pages, internal report, AST Grenoble Lab, Grenoble, France, 2003. Extended to user manual (with examples), 200 pages, 2004.

[4] M.D. Grammatikakis, M. Coppola, S. Curaba, G. Marrucia, and F. Papariello, "OCCN user manual - v1.0.1", 68 pages, internal report, AST Grenoble Lab, Grenoble, France, 2003. Open source SystemC-based modeling library used by many Universities and Industry, see collaborators at http://occn.sourceforge.net

[5] M.D. Grammatikakis, M. Coppola, S. Curaba, G. Marrucia, and F. Papariello, "OCCN v1.0 - White paper", 33 pages, internal report, AST Grenoble Lab, Grenoble, France, 2003.

[6] M.D. Grammatikakis, "Licensing issues for OCCN ", 5 pages, internal report, AST Grenoble Lab, Grenoble, France, 2002.

[7] M.D. Grammatikakis, M. Coppola, S. Curaba and G. Maruccia, "Reference Manual - IPSIM v2.12+", 160 pages, internal report, AST Grenoble Lab, Grenoble, France, 2002. Different versions used by at least three *ST Microelectronics* Corporate Product Divisions.

[8] M.D. Grammatikakis, M. Coppola, S. Curaba and G. Maruccia, "User Manual - IPSIM v2.12+", 50 pages, internal report, AST Grenoble Lab, Grenoble, France, 2002. Various versions, used by at least three *ST Microelectronics* Corporate Product Divisions.

[9] M.D. Grammatikakis, "Guidelines for writing IT specs", internal manuscript, ISD, 2000.

[10] M.D. Grammatikakis, "Specifications of a middleware monitoring service", *Eurescom* project - *P924* deliverable, 2000.

[11] M.D. Grammatikakis, "VPN validation and service level assessment of the *EuroSkyWay* satellite network: Part I: Traffic Models for Basic Applications and Part II: Validation and Emulation Process", internal manuscripts, *EU TEN/TELECOM* project - *REVENUES*, 2000.

[12] M.D. Grammatikakis, "Specifications of an ATM network performance simulation tool", internal project report, Intracom, 2000.

[13] M.D. Grammatikakis, "Research on network simulation", project report, FZI, Juelich, Germany, 1999.

[14] M.D. Grammatikakis, A. David and M. Kraetzl, "Software implementation of concurrent remote enqueues on *Cray-T3E*", unpublished manuscript, 1999.

COURSE NOTES (IN GREEK)

[1] M.D. Grammatikakis, G. Kopidakis, M. Papadakis, and S. Stamatiades, "An Introduction to Numerical Analysis", Dept. Material Science and Technology, University of Crete, 2008

CITATIONS

Although emphasis is on system development, where work is revealed in terms of prototypes, large scale trials and successfull industrial projects, there is also strong evidence of world class excellence in R&D. More specifically, there are **674 citations** to my recent papers in Google Scholar. There are also citations in more than 50 PhD dissertations and hundreds of industry-related sites and electronic magazine articles on state-of-the-art SoC/NoC projects.

RECOGNITION: SCHOLARSHIPS, AWARDS AND HONORS

Industrial Award

Recognition for participation in the open source "*On−chip Communication Network* which won the *ST Microelectronics Corporate Community of Practice Gold Medal Award* in 2005.

Honored and recognized

Who *Who in Science* and *Engineering*, 6th and 7th editions, 2002-2004.

IBC *Eminent Scientists of Today*, 1st edition, 2002.

Teaching/Research Assistantship, University of Oklahoma, 1984-1985, and 1988-1991.

Top graduating senior, University of Crete, Heraklion, Greece, June 1983.

Fellow, National Fellowship Foundation of Greece, 1980-82.

Honorary awards, 1979 National college entrance examinations (rated 1st, University of Crete, Heraklion).

PROFESSIONAL ACTIVITIES

Tutorial

2011, *DATE* tutorial on "On-chip interconnect for new generation of SoC" (with M. Coppola). Participants: ARM, Columbia University, Infineon, Intel and ST Microelectronics.

Member, International Program Committee

2007 to 2010, *DATE*, Task A8: "Application Design".
2006, *DATE*, Task A4: "Secure Systems".
2001-2003, *DATE*, Task D on "Platform Design and VC Reuse Methods".
1998-2004, *Euro Media*, Task: "Communication Technology",

Organizing Chair

Medea+ ToolIP kickoff meeting and 2-day internal Workshop, Heraklion, Greece, May 2001. Facilitated meetings among decision makers, project leaders and participants.

Training workshop on "Design tools for the BBNT gateway, Heraklion, Greece, April 2001. Contributed to success of this 3-day expert-level hands-on training workshop on IP modeling.

Program Chair

Workshop on Intelligent Solutions in Embedded Systems (WISES), Heraklion, Greece, July 2010.
Workshop on Intelligent Solutions in Embedded Systems (WISES), Ancona, Italy, July 2009.
Euro Media conference, London, UK, December 1996.

Medea+ Working Group

Responsible for updating the Medea+ EDA Roadmap chapter on *IP Reuse* (2005 and 2008).

Review

International conferences, such as *DAC, DATE, ISCA, EuroPar, and ParCo*.
Journals, such as *IEEE Trans., JPDC, J. Syst. Arch., Par. Comput., Networks, IPL, and PPL*.

PLATFORMS AND SOFTWARE

Conventional systems, old to new: *UNIVAC* (*NOS OS*), *PDP* 11/70, *VAX* 11/780, *IBM* 4381-2 (*VM*/*CMS*), *IBM*/*PC* (*MS* − *DOS*), *Mac* (*APPLE* − *DOS*), *Tek* 4082, *Sun*, *Sparc*, *Ultrasparc*, and *DEC* Alpha. *UNIX*, *Windows*, *Linux* (*Suse*, *Redhat*, *Fedora Core*, *Slack*) and *Solaris* 10.

Supercomputers, with 8 to 1024 processing elements; from old to new: *HEP* (*Denelcor*'s first ever commercial multicomputer system), *Cyber* − 205 (fastest vector supercomputer available), *Multimax* (multitasking system with concurrent *Pascal* support), *Alliant* − *FX*/8 (with *C* and *Fortran*, *Cray* libraries and *UNIX OS*), *MasPar* − *I* (parallel *C* and *UNIX OS*), *TM* − *CM*5 (data parallel C*, communication libraries, such as *CMMD*, *MPI* and *PVM*, *CMOST OS*), and *Cray* − *T*3*D* & *T*3*E* (*UNICOS OS*).

Embedded Systems, *ARMv*7 (*Odroid XU*3, *XU*4, *Zedboard*/*Zynq*), *ARMv*8 (*Dragonboard* 410*c*, *HiKey*, *Raspberry Pi*2/3, mezzanine sensor boards, sensors/adaptors. *I*2*C*/*SPI* and wireless debug boards (*Beagle I*2*C*/*SPI*, *HackRF*). Experience with *ARM Trustzone*, secure/crypto authentication chips, e.g. *Secure* from 96 *boards*, *AT*88*CKECC* − *AWS* − *XSTK*, *AT*88*CK*590 *Atmel* from *Microchip Technologies*. Smart Vehicles: platform development, *CAN* bus dianostics and security extensions, e.g. using *ECUSim*, *DFRobots CAN* controllers, transceivers, *Gingko* devices. Hybrid/heterogeneous systems, e.g. sensors and *RTOS*, and bare metal. Real-time systems (*Renesas Synergy*, *R* − *Car H*3). Open *RTOS* software, e.g. *FreeRTOS*. *Arduino* microcontroller and shields (*CAN*, *DSP*, *sensors*). Small protocol stacks (*protothreads*, *protosockets*, *uip*, *lwip*). *VivadoHLS* for hardware design.

Sequential programming languages: *C*, *C* + +, *PASCAL*, *Python*, *FORTRAN*, *ADA*, and *BASIC*, working knowledge of *COBOL*, *LISP*, *PROLOG*, *PL*/*I*, assembly for *x*86, *ARM*.

Parallel programming languages and libraries: data parallel *C**, parallel *C*, *HP Fortran*, *Fortran* 90, *Open* − *MP*, *CM Fortran*, *MPI* + *C*, *SCI* ringlets, *Cray ShMem* library, and parallel I/O programming. Development of custom NoC-specific derivative tools based on partitioning/mapping (e.g. *Metis*, *Scotch*), and graph analysis (*nauty*). Working knowledge with *OpenCL*, *Rodinia* benchmarks.

Graphical interface design: expertise in low level *X* − *Windows* programming for efficient *GUI* design for real-time, knowledge of widgets, *Tk* and related statistical and waveform viewing software (*vcd*).

System/Network programming: *IPC*, *UNIX*/*POSIX* shared memory, message passing and thread libraries, synchronization, socket libraries/options, *CORBA*.

Linux kernel programming: system configuration, device drivers, kernel modules (bandwidth regulation, firewall), Linux scheduler (e.g. new weighted RR scheduler).

Simulation and analysis tools: development of custom libraries, e.g. *IPSim* kernel, or general-purpose *GPSS*, *SLAM*, *SAS*, *OMNET*, and *OPNET*. Advanced visualization tools, such as *AVS*, *neato*, and *dotty*. Customized application task generation facilities (e.g. through *TGFF*).

System-on-Chip and IP modeling: expertise in the design and use of electronic system level design automation design languages, e.g. *ST Microelectronics IPSIM* and *OCCN*, and tools based on the *SystemC* design language and extensions, e.g. *SystemC – AMS*, *SystemC – TLM*, *Synopsys CocentriC Studio*. Limited working experience with hardware description languages, such as Verilog and programming language interface (PLI_).
Software tools: *Lex*, *Yacc*, *Lotus*, *Excel*, *Lindo*, *C shell* script, *dinotrace*, *doxygen*, *doc++*, *gnuplot*, *gtkwave*, *mpeg*, *xanim*, *xfig*, *xv*, *xmgrace*, *LaTex*, *troff/nroff*, *mkdoc*, *MS* Office, *MS* Project and *Adobe PS*.
Software installation experience with public domain (*GNU*) compilers, debuggers, communication interfaces. Experience with parallel software tools on clusters of workstations.
General package installation: working experience on *autoconf*, *automake*, *jam*, versioning systems (*cvs*, *svn*, *git*), run-test environments and regression testing. Solaris Studio experience.